CLAIMS

1. A method of fabricating a transistor which comprises the steps of:

(a) providing a semiconductor substrate having a first source/drain region and a second source/drain region therein; and

(b) providing a channel region between said first and second source/drain regions in said substrate having a first dopant profile in a first region substantially in said channel region and a second dopant profile different from said first dopant profile in a second region substantially between the first region and said first source/drain region, the second dopant profile comprising an implant substantially bounded between said first region and said first source/drain region.

2. The method of claim 1 wherein said channel region is formed by implanting a dopant providing a relatively high V_T dopant profile adjacent to said first source/drain region and implanting a dopant providing a relatively low dopant profile adjacent to said second source/drain region.

3. The method of claim 1 wherein said channel region is formed by implanting a dopant providing a relatively low V_T dopant profile along said channel and then selectively implanting a dopant providing a relatively high V_T dopant profile adjacent to said first source/drain region.

4. The method of claim 2 wherein said channel region is formed by implanting a dopant providing a relatively high V_T dopant profile adjacent to said first source/drain region and implanting a dopant providing a relatively low dopant profile adjacent to said second source/drain region.

5. The method of claim 2 wherein said channel region is formed by implanting a dopant along the entire channel and then selectively implanting a dopant providing a relatively high V_T dopant profile of opposite conductivity type only adjacent to said first source/drain region to provide a net relatively high V_T region only adjacent to said first source/drain region

6. A method of fabricating a transistor which comprises the steps of:

(a) providing a semiconductor substrate having source and drain regions therein; and

(b) providing a channel region between said source and drain regions in said substrate having a dopant providing a relatively low V_T dopant profile central region between said source and drain regions and regions in said channel region between said source region and said central region and between said drain region and said central region having a dopant providing a relatively high V_T dopant profile.

7. The method of claim 6 wherein said channel region is formed by implanting a dopant having a relatively low V_T dopant profile intermediate said source and drain regions and implanting a dopant having a relatively high V_T dopant profile adjacent to said source and drain regions.

8. The method of claim 6 wherein said channel region is formed by implanting a dopant having a relatively low V_T dopant profile along said channel and then selectively implanting a dopant having a relatively high V_T dopant profile adjacent to said source region.

9. A transistor which comprises:

(a) a semiconductor substrate having source and drain regions therein; and

(b) a channel region between said source and drain regions in said substrate having a relatively low V_T central region between said source and drain regions and relatively high V_T regions adjacent to said source and drain regions.

10. The transistor of claim 9 wherein said channel region is an implanted low V_T dopant intermediate said source and drain regions are an implanted high V_T dopant adjacent said source and drain regions.

11. The transistor of claim 9 wherein said channel region is an implanted relatively low V_T dopant along said channel and a selectively implanted relatively high V_T dopant adjacent to said source region.

12. A method of fabricating a transistor which comprises the steps of:

(a) providing a substrate;

(b) providing a first mask layer over said substrate, said first layer having a trench extending therethrough to said substrate;

(c) forming sidewalls in said trench with a material different from said first mask layer; and

(d) performing an implant into said substrate through said trench, said layer providing a mask to said implant external of said trench.

13. The method of claim 12 further including the step of removing a portion of said sidewall prior to performing said implant.

14. A method of fabricating a transistor which comprises the steps of:

(a) providing a substrate;

(b) providing a first mask layer over said substrate, said first layer having a trench extending therethrough to said substrate;

(c) forming sidewalls on said trench with a sidewall material different from said first mask layer;

(d) filling the space bordered by said sidewalls with a filling material different from said sidewall material;

(e) removing at least a portion of said sidewalls while retaining at least a portion of said filling material; and

(f) performing an implant into said substrate through said trench, said layer, said filling material and any remaining sidewall providing a mask to said implant external of said trench.

15. A transistor which comprises:

(a) a semiconductor substrate having a first source/drain region and a second source/drain region therein;

(b) a channel region between said first and second source/drain regions;

(c) a gate dielectric disposed outwardly from said channel region;

(d) a gate electrode disposed outwardly from said gate dielectric; and

(e) a dopant in said substrate comprising an implant aligned with said gate contained substantially within a projection of said gate electrode to said substrate, the projection of the area of the implant to the surface of the substrate being less than the projection of the gate.

16. A method of fabricating a transistor which comprises the steps of:

(a) providing a substrate;

(b) providing a first layer of said substrate, said first layer having a trench for formation of a gate;

(c) forming a sidewall within said trench; and

(d) performing a first implant into said substrate, said first implant being partially masked by said sidewall.

17. The method of claim 16 wherein a portion of said sidewall is removed prior to said first implant.

18. The method of claim 16 further including performing a second implant into said substrate which is not masked by said sidewall.

19. The method of claim 18 wherein said second implant is performed prior to formation of said sidewall.

20. The method of claim 18 wherein said second implant is performed after removal of said sidewall.

21. The method of claim 16 further including the steps of:

(e) filling any space adjacent said sidewall;

(f) planarizing the surface of the structure being fabricated; and

(g) removing a portion of said sidewall.

22. The transistor of claim 15 wherein one edge of said implant region is substantially aligned with one edge of said gate electrode and the opposite edge of said implant region is within the projection of the gate electrode.

23. A transistor which includes:

(a) a substrate;

(b) a gate electrode disposed over said substrate; and

(c) a punch through implant in said substrate contained within a projection of said gate electrode.